English Translation of JP 04-313729

(19) Japan Patent Office (JP)

(12) Publication of Laid-Open Patent Application (A)

(11) Publication No. 4-313729

(43) Publication Date: November 5, 1992

(51) Int. Cl. 5 Identification Mark Office Reference Number FI

Α

G02F 1/1343

9018-2K

1/136 500

9018-2K

H01L 27/12 21/336 8728-4M

9056-4M

H01L 29/78 311P

Display Location of technique

Request for Substantive Examination: Not requested

Number of Claims: 1

(Total 6 pages)

Continue to the last page

(21) Application No. 3-76069

(22) Filing Date: April 9, 1991

(71) Applicant: 000006013

Mitsubishi Electric Corporation

2-2-3, Marunouchi, Chiyoda-ku, Tokyo

(72) Inventor: Akira Kawamoto

c/o Material Laboratory of Mitsubishi Electric Corporation

8-1-1, Tsukaguchi hon-machi, Amagasaki-shi, Hyogo

(74) Agent: Patent Attorney Mamoru Takada (and one other)

# (54) [Title of the Invention]

Liquid Crystal Display Device

## (57) [Abstract]

[Object] To obtain a liquid crystal display device in which the resistance of a gate wiring

is lowered without adding one layer of the gate wiring.

[Structure] It is characterized that a gate electrode and a source electrode wiring are formed in the same one layer; a source electrode, a drain electrode, and a gate electrode wiring are formed in another layer; the gate electrode and the gate electrode wiring, and the source electrode and the source electrode wiring are each connected through a contact hole.

[Effect] The resistance of the gate wiring can be lowered by using a low-resistant material for the gate electrode wiring.

[Scope of Claim]

[Claim 1] A liquid crystal display device comprising:

- a thin film transistor array substrate including:
- a plurality of gate electrodes which are provided to be attached to a source electrode wiring over a transparent insulating substrate and which are connected to the source electrode wiring in each pixel,
  - a plurality of source electrodes which intersect with the gate electrodes,
- a gate electrode wiring which is provided to be attached to the source-drain electrode and which is connected to the source electrode in each pixel, and
- a pixel electrode which is provided at the intersection of the gate electrode and the source electrode and which is connected to the drain electrode of a thin film transistor including the gate electrode and the source-drain electrode;

an opposite electrode substrate which is provided to be opposed to the thin film transistor array substrate; and

a liquid crystal display material which is interposed between the opposite electrode substrate and the thin film transistor array substrate.

[Detailed Description of the Invention]

[0001]

[Industrial Field of the Invention]

The present invention relates to a liquid crystal display device which includes a wiring structure which allows the resistance of a gate wiring to lower to be high quality in a liquid crystal display device using a TFT (Thin Film Transistor) array substrate.

[0002]

[Prior Art] A liquid crystal display device is normally structured by a method in which a display material such as a liquid crystal is interposed between two substrates which are opposed to each other and voltage is applied to the display material. In this case, a pixel electrode arranged in matrix form is provided over at least one of the substrates, and an active element having non-linear characteristics such as a field effect transistor (FET) is provided in each pixel to selectively operate the pixel. In addition, a charge retention capacitor is provided in each pixel to improve image quality.

[0003] FIG. 6 is a plain view showing a pixel of a TFT array substrate used for a conventional liquid crystal display device, for example, that is disclosed in Japanese Patent Application Laid-Open No. 64-26822, FIG. 7 is a cross-sectional view showing a cross-section taken along a line A-A of FIG. 6, and FIG. 8 is an equivalent circuit diagram of FIG. 6.

[0004] In FIGS. 6 to 8, the reference numeral 1 denotes a source electrode wiring, the reference numeral 2 denotes a gate electrode wiring formed over a transparent insulating substrate 14, the reference numeral 3 denotes a gate electrode wiring of the next stage formed over the transparent insulating substrate 14, the reference numeral 4 denotes a gate insulating film, the reference numeral 5 denotes a hydrogenated amorphous silicon i layer, the reference numeral 7 denotes a hydrogenated amorphous silicon n\* layer, the reference numeral 8 denotes a drain electrode, the reference numeral 9 denotes a pixel electrode, the reference numeral 10 denotes a protective film, the reference numeral 18 denotes a charge retention capacitor, the reference numeral 19 denotes a gate wiring of Al, the reference numeral 35 denotes a liquid crystal, and the reference numeral 38 denotes an opposite electrode

[0005] As the structure of FIGS. 6 and 7, the gate electrode wiring 2 and the gate electrode wiring 3 are formed from Cr over the transparent insulating substrate 14. Moreover, the gate wiring 19 of Al is formed over the gate electrode wiring 3.

[0006] Then, the gate insulating film 4 is formed, and then, a TFT is structured with the source electrode wiring 1 and the drain electrode 8, along with forming the semiconductor film 5 over the gate insulating film 4, and a TFT array is structured with the TFT and the

pixel electrode 9.

[0007] The above stage of the gate electrode wiring 3 and the pixel electrode 9 are overlapped with each other so as to interpose the gate insulating film 4 to form the charge retention capacitor 18, by utilizing next or previous row of the gate electrode wiring 3 in which electric potential is fixed except the case in which the gate electrode wiring 3 is scanned.

[0008] A liquid crystal display device is constituted by interposing a liquid crystal or the like between the TFT array substrate and the opposite electrode substrate having a color filter and a transparent conductive film.

#### [0009]

[Problems to be solved by the Invention] The conventional liquid crystal display device is structured as described above; thus, a layer of a gate wiring added to lower the resistance of the gate wiring. Therefore, there are problems that the number of steps increases, the manufacturing cost increases, and a yield is lowered.

[0010] The present invention is made to solve the conventional problems as described above, and it is an object of the present invention to provide a liquid crystal display device in which the cost can be lowered, a yield can be improved, and the resistance of wiring can be lowered without increasing the layer structure.

#### [0011]

[Means for Solving the Problem] A liquid crystal display device according to the present invention is provided with a gate electrode and a source electrode wiring formed in the same one layer and a source-drain electrode and a gate electrode wiring formed in another layer.

### [0012]

[Operation] The gate electrode wiring of the present invention is formed from a material for a source-drain electrode; therefore, a material having low resistivity such as Al or an alloy of Al can be used, and the resistance of the gate wiring can be lowered.

### [0013]

[Embodiment] Hereinafter, an embodiment of the present invention is described with reference to figures. FIG. 1 is a plain view showing a pixel of a TFT array substrate of a liquid crystal display device according to one embodiment of the present invention, FIG. 2 is a cross-sectional view showing a cross-section taken along a line B-B of FIG. 1, and FIG. 3 is an equivalent circuit diagram of FIG. 1.

[0014] Through FIGS. 1 to 3, the same or corresponding parts are denoted by the same reference numerals of FIGS. 6 to 8. In FIGS. 1 to 3, the reference numeral 1 denotes a source electrode wiring over a dielectric film 13 formed over a transparent insulating substrate 14 to be connected to a source electrode 1A.

[0015] A gate electrode 2A is formed over the dielectric film 13, and the gate electrode 2A is connected to a gate electrode wiring 2. A gate electrode 3A in an above stage or a next stage is formed over the dielectric film 13, and a gate electrode wiring 3 is connected over the gate electrode 3A.

[0016] Moreover, a pixel electrode 9 is formed over the dielectric film 13, and the pixel electrode 9 is connected to a drain electrode 8. A gate insulating film 4 is formed over the source electrode wiring 1, the gate electrode 2A, the pixel electrode 9, the gate electrode 3A in a previous row or a next row, and the dielectric film 13. In addition, a semiconductor i layer 5 is formed over the gate insulating film 4, and an upper insulating film 6 is formed over the upper surface thereof. After patterning the upper insulating film 6, a semiconductor n layer 7 is formed.

[0017] The gate insulating film 4, the semiconductor i layer 5, and the upper insulating film 6 are opened to form contact holes 23 to 27.

[0018] The pixel electrode 9 is connected to the drain electrode 8 through the contact hole 23, and the source electrode wiring 1 is connected to the source electrode 1A through the contact hole 24. As apparent from FIG. 1, the gate electrode wiring 2 is connected to the gate electrode 2A through the contact hole 27. A protective film 10 is formed over the top surface.

[0019] Note that the reference numeral 12 denotes a floating electrode formed over the transparent insulating substrate 14, and as shown in FIG. 3, the reference numeral 15 denotes a TFT, the reference numeral 16 denotes a gate-source parasitic capacitor, the reference numerals 21 and 22 denote a charge retention capacitor, the reference numeral 35 denotes a liquid crystal, and the reference numeral 38 denotes an opposite electrode.

[0020] Next, a procedure of manufacturing process of this embodiment according to the present invention is described. First, a transparent conductive film such as ITO is deposited over the transparent insulating substrate 14 such as glass by an EB (Electron Beam) evaporation method, a sputtering method, or the like. Then, the floating electrode 12 is formed in an island-shape by a method such as photolithography, etching, or the like. [0021] Next, the dielectric film 13 is formed from silicon nitride, silicon oxide, or tantalum oxide, or two or more layers of them by a plasma CVD method, a sputtering method, or the like.

[0022] Then, a transparent conductive thin film such as ITO is formed by a sputtering method or the like. And then, the pixel electrode 9 is formed from the transparent conductive thin film by photolithography, etching, or the like. At this time, the floating electrode 12 and the pixel electrode 9 are overlapped with each other by interposing the dielectric film 13 therebetween to form the charge retention capacitor 21.

[0023] Next, a metal such as Cr or Mo is deposited over the dielectric film 13 by using a sputtering method or the like. Then, the gate electrode 2A, the gate electrode 3A in an above stage or a next stage, and the source electrode 1A are formed by photolithography, etching, or the like. At this time, the floating electrode 12 and the gate electrode 3A are overlapped to each other by interposing the dielectric film 13 therebetween to form the charge retention electrode 22.

[0024] Next, the gate insulating film 4 such as silicon nitride, the semiconductor i layer 5 such as hydrogenated amorphous silicon i layer, and the upper insulating film 6 are sequentially deposited by a plasma CVD method or the like.

[0025] Then, the upper insulating film 6 is patterned, then, a semiconductor n\* layer 7 such as a hydrogenated amorphous silicon n\* layer is formed by a plasma CVD method or the like, and then, the contact hole 23 which connects the pixel electrode 9 and the drain electrode 8, the contact hole 24 which connects the source electrode wiring 1 and the source electrode 1A, and the contact hole 27 which connects the gate electrode 2A and the gate electrode wiring 2 are formed.

[0026] Next, a barrier metal such as Cr and a conductive thin film such as Al or Mo are deposited by a sputtering method or the like, and are then patterned into the source electrode 1A and the drain electrode 8.

[0027] Moreover, the unnecessary semiconductor n\* layer 7 and the semiconductor i layer 5 are etched off by dry etching or the like. Then, finally, a silicon nitride film, a silicon oxide film, or tantalum pentoxide is deposited by a plasma CVD method, a sputtering method, or the like, and then are patterned to form the protective film 10.

[0028] A liquid crystal display material such as the liquid crystal 35 is interposed between the TFT array substrate formed as described above and an opposite electrode substrate having a transparent electrode, a color filter, and the like; thus, a liquid crystal display device is manufactured.

[0029] Note that the case where a transparent conductive film is used as the floating electrode 12 is described in the above embodiment, but an opaque conductive film such as a metal film may be used, if it has no difficulty in displaying.

[0030] Moreover, in the above embodiment, the case where the upper insulating film 6 is used in the TFT constitution is shown, but a TFT structure in which the upper insulating film is not used in the TFT constitution shown in the plain view of FIG. 4 and FIG. 5 (a cross-sectional view taken along a line C-C of FIG. 4) may be employed.

[0031] Note that the reference numeral 17 shown in FIG. 5 denotes a light shielding film formed over the protective film 10 in the TFT constitution.

[0032]

[Effect of the Invention] As described above, according to the present invention, the source and drain electrode and the gate electrode wiring are formed in the same one layer, along with forming the gate electrode and the source wiring in another same layer. In addition, the gate electrode and the gate electrode wiring 2, and the source electrode and the source electrode wiring 1 are connected to each other through the contact hole, respectively. Therefore, a gate wiring can be formed from a source-drain electrode material

[0033] Therefore, the present invention has such an effect that the resistance of the gate electrode wiring can be lowered by using a low resistant material such as Al for the source-drain electrode material.

[Brief Description of the Drawings]

- [FIG. 1] A plain view showing a pixel of a TFT array substrate of a liquid crystal display device according to one embodiment of the present invention.
- [FIG. 2] A cross-sectional view showing a cross-section taken along a line B-B of FIG. 1.
- [FIG. 3] An equivalent circuit diagram of FIG. 1.
- [FIG. 4] A plain view showing a pixel of a TFT array substrate of a liquid crystal display device according to another embodiment of the present invention.
- [FIG. 5] A cross-sectional view showing a cross-section taken along a line C-C of FIG. 4.
- [FIG. 6] A plain view showing a pixel of a TFT array substrate used for a conventional liquid crystal display device.
- [FIG. 7] A cross-sectional view showing a cross-section taken along a line A-A of FIG. 6.
- [FIG. 8] An equivalent circuit diagram of FIG. 6.

#### [Description of the Numerals]

- 1 source electrode wiring
- 1A source electrode
- 2, 3 gate electrode wiring
- 2A, 3A gate electrode
- 4 gate insulating film
- 5 semiconductor i laver
- 6 upper insulating film
- 7 semiconductor n<sup>+</sup> layer
- 8 drain electrode
- 9 pixel electrode
- 10 protective film
- 12 floating electrode
- 13 dielectric film
- 14 transparent insulating substrate
- 15 TFT
- 16 parasitic capacitor
- 17 light shielding film
- 21, 22 charge retention capacitor

23-27 contact hole

35 liquid crystal

38 opposite electrode

[Amendment]

[Date submitted] October 30, 1991

[Amendment 1]

[Document Amended] Specification

[Item Amended] Scope of Claim

[Method of Amendment] Modification

[Contents of Amendment]

[Scope of Claim]

[Claim 1] A liquid crystal display device comprising:

- a thin film transistor array substrate including:
- a plurality of gate electrodes which are provided to be attached to a source electrode wiring over a transparent insulating substrate and which are connected to the gate electrode wiring in each pixel.
  - a plurality of source electrodes which intersect with the gate electrodes,
- a gate electrode wiring which is provided to be attached to the source-drain electrode and which is connected to the gate electrode in each pixel, and
- a pixel electrode which is provided at the intersection of the gate electrode and the source electrode and which is connected to the drain electrode of a thin film transistor including the gate electrode and the source-drain electrode;
- an opposite electrode substrate which is provided to be opposed to the thin film transistor array substrate: and
- a liquid crystal display material which is interposed between the opposite electrode substrate and the thin film transistor array substrate.

[Amendment 2]

[Document Amended] Specification

[Item Amended] 0020

[Method of Amendment] Modification

Content of Amendment

[0020] Next, a procedure of manufacturing process of this embodiment according to the present invention is described. First, a transparent conductive film such as ITO is deposited over the transparent insulating substrate 14 such as glass by an EB (Electron Beam) evaporation method, a sputtering method, or the like. Then, the floating electrode 12 is formed in an island-shape by a method such as photoengraving, etching, or the like.

[Amendment 3]

[Document Amended] Specification

[Item Amended] 0022

[Method of Amendment] Modification

[Content of Amendment]

[0022] Then, a transparent conductive thin film such as ITO is formed by a sputtering method or the like. And then, the pixel electrode 9 is formed from the transparent conductive thin film by <a href="https://photoengraving">photoengraving</a>, etching, or the like. At this time, the floating electrode 12 and the pixel electrode 9 are overlapped with each other by interposing the dielectric film 13 therebetween to form the charge retention capacitor 21.

[Amendment 4]

[Document Amended] Specification

[Item Amended] 0023

[Method of Amendment] Modification

[Contents of Amendment]

[0023] Next, a metal such as Cr or Mo is deposited over the dielectric film 13 by using a sputtering method or the like. Then, the gate electrode 2A, the gate electrode 3A in an above stage or next stage, and the source electrode wiring 1A are formed by photoengraving, etching, or the like. At this time, the floating electrode 12 and the gate electrode 3A are overlapped to each other by interposing the dielectric film 13 therebetween to form the charge retention electrode 22.

[Amendment 5]

[Document Amended] Specification

[Item Amended] 0026

[Method of Amendment] Modification

[Contents of Amendment]

[0026] Next, a barrier metal such as Cr and a conductive thin film such as Al or Mo are deposited by a sputtering method or the like, and are then patterned into the gate electrode wirings 2 and 3, the source electrode 1A and the drain electrode 8.

Continuation of the front page

(51) Int. Cl.<sup>5</sup> Identification Mark Office Reference Number FI H01L 29/784

Display Location of technique